Arief Wicaksana

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Zurich, Switzerland

SKILLS

HARDWARE DEVELOPMENT
- FPGA design and prototyping, IP development using VHDL/Verilog/SystemVerilog, Hardware emulation, ARM CPU microarchitecture, High-Level Synthesis, Bus Functional Model

SOFTWARE DEVELOPMENT
- Virtual prototyping, development in C++/SystemC-TLM, Python/Perl/Bash/Tcl scripting, Linux, Object-Oriented Programming

PROJECT MANAGEMENT
- Agile methodology, JIRA, collaborative development using git, weekly reports, gap and risk analysis

LEADERSHIP
- Teamwork, communication, great interpersonal skills, attention to detail, fast learner, assertive

EXPERIENCES

SENIOR R&D ENGINEER (ARCHITECT) | HUAWEI TECHNOLOGIES
December 2021 - Present | Zurich, CH
- Performed architecture exploration, algorithm evaluation and preliminary performance and cost evaluation of DSP accelerator design for communication system

SENIOR CPU PERFORMANCE ANALYSIS ENGINEER | ARM
July 2020 - December 2021 (1.5 years) | Sophia Antipolis, FR
- Performed CPU performance verification through emulation and cycle-accurate simulation and analyzed CPU design at microarchitecture level to fix performance bug
- Provided weekly performance regression reports and statistics in ARM CPU core development projects
- Developed automated performance verification flow to reduce error and increase engineering productivity

RESEARCH ENGINEER | CEA LIST
November 2018 - June 2020 (1.5 years) | Paris, FR
- Developed virtual prototyping tool in SystemC/C/C++ language for early validation and Design Space Exploration in SoC development
- Applied code annotation in QEMU for performance verification and estimation purposes
- Developed and integrated custom neural network processor simulator in virtual prototyping co-simulation
- Contributed in simulation and performance verification work package in H2020 project

JUNIOR RESEARCHER | TIMA LABORATORY (CNRS/UGA/G-INP)
October 2015 - November 2018 (3 years) | Grenoble, FR
- Developed communication method to support hardware context-switch on FPGA platforms with different families and vendors
- Built framework enabling runtime task migration between heterogeneous FPGAs to virtualize processing nodes in cloud environment
- Published articles in peer-reviewed journal and international conferences (ACM and IEEE)

EDUCATION

PH.D., COMPUTER SCIENCE | UNIV. GRENOBLE ALPES
2015 - 2018
- Thesis: Portable Infrastructure for Heterogeneous Reconfigurable Devices in a Cloud-FPGA Environment

ENGINEER, EMBEDDED SYSTEMS | UNIV. GRENOBLE ALPES
2013 - 2015 | Graduated with distinction

BACHELOR, ELECTRICAL ENGINEERING | ITB
2007 - 2011 | Graduated with distinction

INTERESTS

LANGUAGES | English, French, Indonesian, German(beginner)
ACTIVITIES | International forum (MPSoC17, MPSoC22), Photography
SPORTS | Volleyball, Ski, Cycling

OTHER EXPERIENCES

CONTRACTUAL LECTURER | **ENSIMAG (GRENOBLE INP)**
September 2016 - August 2018 (2 years) | Grenoble, FR

- Taught architecture and digital processors lab courses
- Prepared course material and exam evaluating student competencies in VHDL and assembly programming

PUBLICATIONS

Wicaksana, Arief, and Arif Sasongko. "Fast and reconfigurable packet classification engine in FPGA-based firewall." In *Proceedings of the 2011 International Conference on Electrical Engineering and Informatics*, pp. 1-6. IEEE, 2011.

Wicaksana, Arief, Adrien Prost-Boucle, Olivier Muller, Frédéric Rousseau, and Arif Sasongko. "On-board non-regression test of HLS tools targeting FPGA." In *Proceedings of the 27th International Symposium on Rapid System Prototyping: Shortening the Path from Specification to Prototype*, pp. 41-47. 2016.

Wicaksana, Arief, Alban Bourge, Olivier Muller, and Frédéric Rousseau. "Demonstration of a context-switch method for heterogeneous reconfigurable systems." In *2016 26th International Conference on Field Programmable Logic and Applications (FPL)*, pp. 1-1. IEEE, 2016.

Wicaksana, Arief, Alban Bourge, Olivier Muller, Arif Sasongko, and Frédéric Rousseau. "Prototyping dynamic task migration on heterogeneous reconfigurable systems." In *2017 International Symposium on Rapid System Prototyping (RSP)*, pp. 16-22. IEEE, 2017.

Bernardeschi, Cinzia, Andrea Domenici, Maurizio Palmieri, Sergio Saponara, Tanguy Sassolas, **Arief Wicaksana**, and Lilia Zaourar. "Cross-level Co-simulation and Verification of an Automatic Transmission Control on Embedded Processor." In *International Conference on Software Engineering and Formal Methods*, pp. 263-279. Springer, Cham, 2020.

Sasongko, Arif, IM Narendra Kumara, **Arief Wicaksana**, Frédéric Rousseau, and Olivier Muller. "Hardware context switch-based cryptographic accelerator for handling multiple streams." *ACM Transactions on Reconfigurable Technology and Systems (TRETS)* 14, no. 3 (2021): 1-25.

Charif, Amir, **Arief Wicaksana**, Salah-Eddine Saidi, Tanguy Sassolas, Caaliph Andriamisaina, and Nicolas Ventroux. "SESAM: A Comprehensive Framework for Cyber–Physical System Prototyping." *Multi-Processor System-on-Chip 2: Applications* (2021): 135-156.

Wicaksana, Arief, Olivier Muller, Frédéric Rousseau, and Arif Sasongko. "Maintaining Communication Consistency During Task Migrations in Heterogeneous Reconfigurable Devices." *Multi-Processor System-on-Chip 1: Architectures* (2021): 255-285.

Jebali, Fatma, Oumaima Matoussi, **Arief Wicaksana**, Amir Charif, and Lilia Zaourar. "Decoupling processor and memory hierarchy simulators for efficient design space exploration." In *System Engineering for constrained embedded systems*, pp. 47-52. 2022.

REFERENCES

Available upon request